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AN ENGINEERING APPROACH TO DIGITAL DESIGN

WILLIAM I. FLETCHER
Utah State University
Logan, Utah

PRENTICE-HALL, INC., *Englewood Cliffs, New Jersey 07632*

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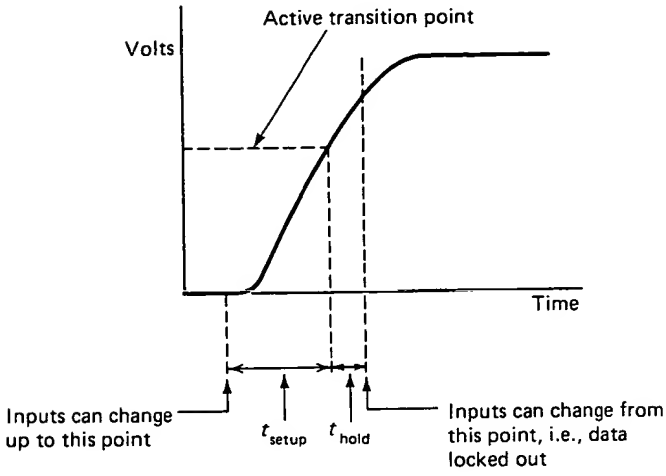
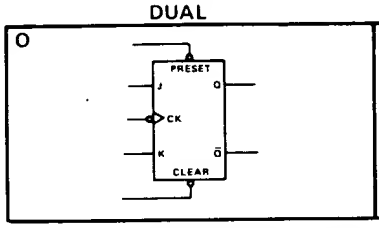


Fig. 5-37. A typical clock waveform for a rising-edge-triggered (RET) device expanded to illustrate the set-up time and the hold time definitions.

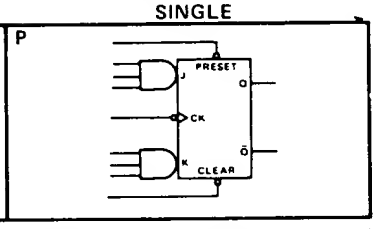
Fig. 5-38. Data sheets and logic diagrams for the SN74110 and SN74111. (Courtesy of Texas Instruments, Inc.)

J-K FLIP-FLOPS WITH DATA LOCKOUT

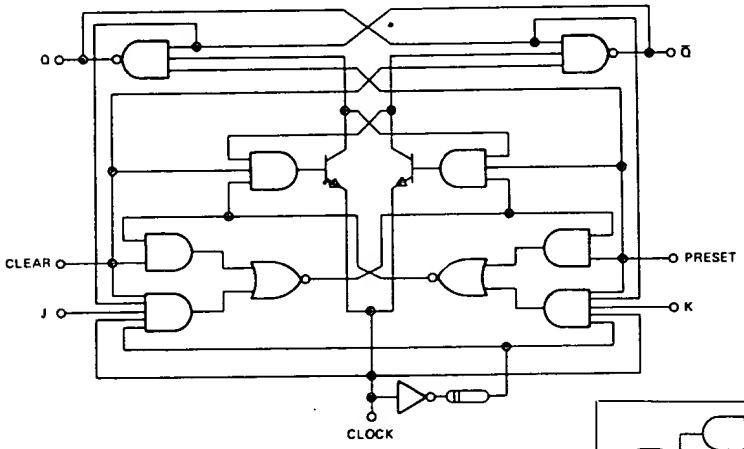
DUAL

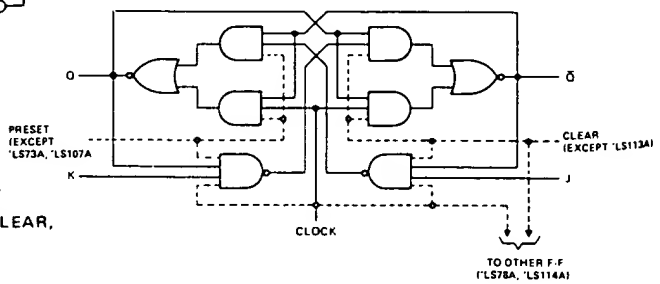


SINGLE



DWG. REF.	TYPICAL CHARACTERISTICS f_{max} (MHz)	Pwr/F·F (mW)	DATA TIMES SETUP (ns)	HOLD (ns)	DEVICE TYPE AND PACKAGE −55 C to 125 C		0 C to 70 C	
O	25	70	0†	30†	SN54111	J, W	SN74111	J, N
P	25	100	20†	5†	SN54110	J, W	SN74110	J, N





'LS73A, 'LS107A—DUAL J-K WITH CLEAR
'LS76A, 'LS112A—DUAL J-K WITH CLEAR AND PRESET
'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
'LS113A—DUAL J-K WITH PRESET

'LS73A, 'LS76A, 'LS78A, 'LS112A, 'LS113A, 'LS114A

† ↓ The arr

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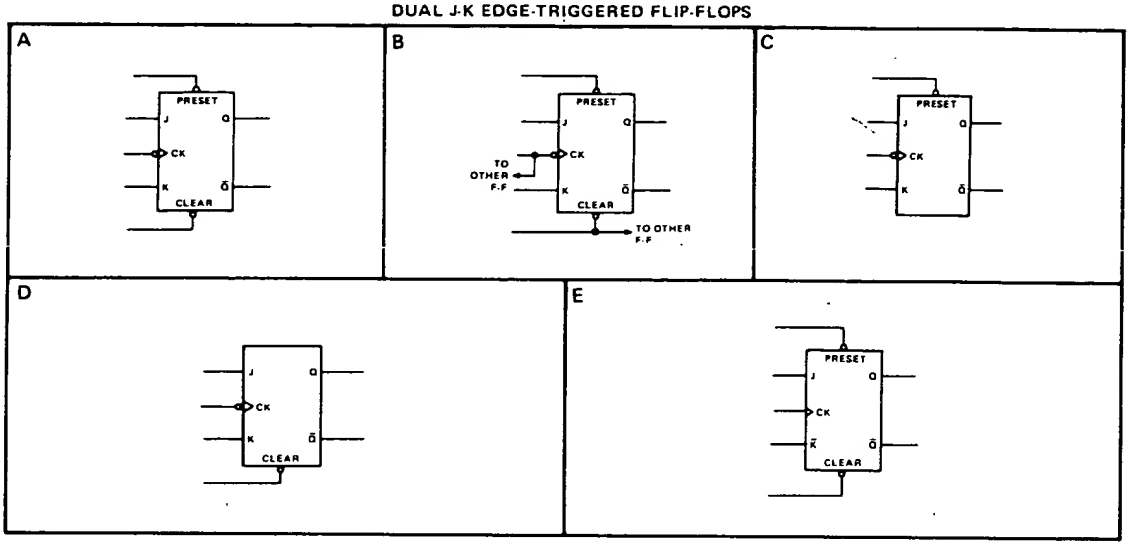
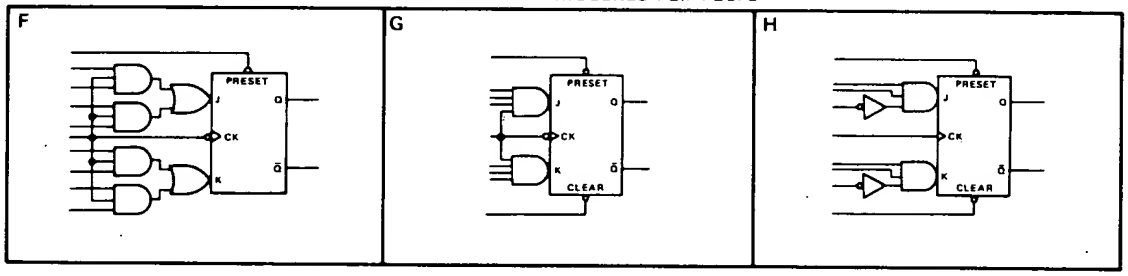
waveform for a device expanded and the hold time

DUAL J-K EDGE-TRIGGERED FLIP-FLOPS



SINGLE J-K EDGE-TRIGGERED FLIP-FLOPS



DWG REF.	TYPICAL CHARACTERISTICS f_{max} (MHz)	Pwr/F-F (mW)	DATA TIMES SETUP (ns)	HOLD (ns)	DEVICE TYPE AND PACKAGE −55°C to 125°C		0°C to 70°C		PAGE REFERENCES PIN ASSIGNMENTS	ELECTRICAL
A	125	75	3↓	0↑	SN54S112	J, W	SN74S112	J, N	5-34	6-58
	50	100	13↑	0↑	SN54H106	J, W	SN74H106	J, N	5-32	6-52
	45	10	20↑	0↑	SN54LS76A	J, W	SN74LS76A	J, N	5-23	6-58
	45	10	20↑	0↑	SN54LS112A	J, W	SN74LS112A	J, N	5-34	6-56
B	125	75	3↓	0↑	SN54S114	J, W	SN74S114	J, N	5-34	6-58
	50	100	13↑	0↑	SN54H108	J, W	SN74H108	J, N	5-32	6-52
	45	10	20↑	0↑	SN54LS78A	J, W	SN74LS78A	J, N	5-24	6-56
	45	10	20↑	0↑	SN54LS114A	J, W	SN74LS114A	J, N	5-34	6-56
C	125	75	3↓	0↑	SN54S113	J, W	SN74S113	J, N	5-34	6-58
	45	10	20↑	0↑	SN54LS113A	J, W	SN74LS113A	J, N	5-34	6-56
D	50	100	13↑	0↑	SN54H103	J, W	SN74H103	J, N	5-31	6-52
	45	10	20↑	0↑	SN54LS73A	J, W	SN74LS73A	J, N	5-22	6-56
	45	10	20↑	0↑	SN54LS107A	J	SN74LS107A	J, N	5-32	6-56
E	33	10	20↑	5↑	SN54LS109A	J, W	SN74LS109A	J, N	5-33	6-56
	33	45	10↑	6↑	SN54109	J, W	SN74109	J, N	5-33	6-46
F	50	100	13↑	0↑	SN54H101	J, W	SN74H101	J, N	5-31	6-52
G	50	100	13↑	0↑	SN54H102	J, W	SN74H102	J, N	5-31	6-52
H	35	65	20↑	5↑	SN5470	J, W	SN7470	J, N	5-21	6-46

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

Fig. 5-39. Data sheet for RET and FET. JK Flip-Flops. (Courtesy of Texas Instruments, Inc.)

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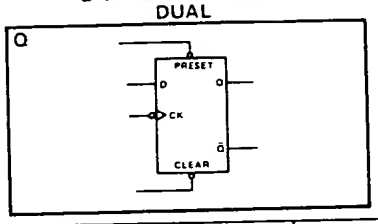
D-TYPE FLIP-FLOPS
DUAL



DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		TEMPERATURE RANGE	
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	−55°C to 125°C	0°C to 70°C
Q	110	75	3†	2†	SN54S74	SN74S74
	43	75	15†	5†	SN54H74	SN74H74
	33	10	25†	5†	SN54LS74	SN74LS74
	25	43	20†	5†	SN5474	SN7474
	3	4	50†	0†	SN54L74	SN74L74

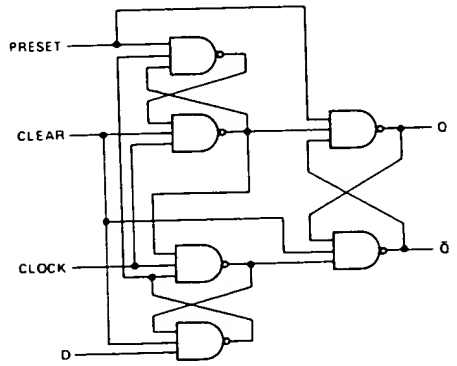


Fig. 5-40. Data and specification sheets for RET D Flip-Flops. (Courtesy of Texas Instruments, Inc.)

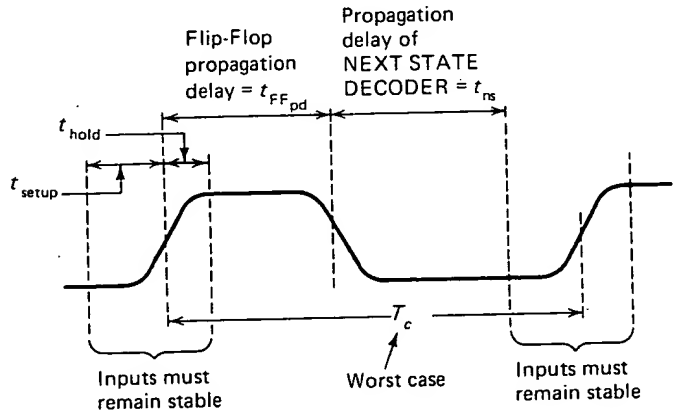


Fig. 5-41. Worst case timing related to maximum clock frequency determination.

The logic diagrams for the devices shown in Figures 5-36, 5-37, 5-38, and 5-39 are vastly different from those developed earlier. The reason for this is twofold:

(1) These devices incorporate the edge-trigger or lock-out features.
(2) The actual integrated circuit manufacturing processes many times dictate a particular logic form.

However, the EXCITATION TABLES for these IC devices are identical to those we have developed. Also, note that the rising-edge of the clock for the SN74111 locks the data into the master cell and the falling-edge transfers this data to the outputs, providing advantages or disadvantages depending on the circumstances.

We see in Chapter 10 how Flip-Flops with edge-triggering and data lock-out features can be designed in a straightforward manner. However, we use these devices and other similar devices to our advantage in the next several chapters to implement a variety of finite-state machines.

5-20 TIMING AND TRIGGERING CONSIDERATIONS

It should be noted that two important timing constraints are listed in the typical data sheet listing shown in Figures 5-38, 5-39, and 5-40. These are SET-UP and HOLD times. The definition of *SET-UP time is the time required for the input data to settle in before the triggering edge of the clock.* If you choose to ignore this specification, you should expect unpredictable behavior. This unpredictable behavior manifests itself in several ways:

(1) missed data or ignored actions;
(2) possible partial transient outputs.

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These partial transient outputs are referred to as "partial SET" and "partial RESET" outputs. In other words, it is possible to start a RESET or SET operation, causing the output to start to change, but to fall back to its original state. Worse yet, a metastable condition can be precipitated in which the Flip-Flop is neither SET nor RESET for some undeterminable time. These concepts are fundamental in nature and are discussed at length in Chapter 7.

The definition of *HOLD time is the time required for the data to remain stable after the triggering edge of the clock.* Again, if you choose to ignore this specification, unpredictable behavior will result.

In keeping with this odd behavior constraint, these critical timing specifications also help determine the maximum allowable clock frequency for a finite-state machine. With all constraints included, Figure 5-41 illustrates how the worst case $t_{SET\text{-}UP}$, t_{HOLD}, Flip-Flop propagation delay and propagation delay of the NEXT STATE DECODER add together to determine the maximum clock frequency.